# Addressing

### General

Signal exchange between module and bus system takes place through a shared memory. This memory buffers arriving telegrams, which are to be received by the module, as well as calculated function results which are to leave the module.

For this reason, the shared memory uses source registers for the telegrams to be sent and sink registers for telegrams to be received. Register numbers 0 to 63 are defined as source registers and register numbers 64 to 199 are defined as sink registers.

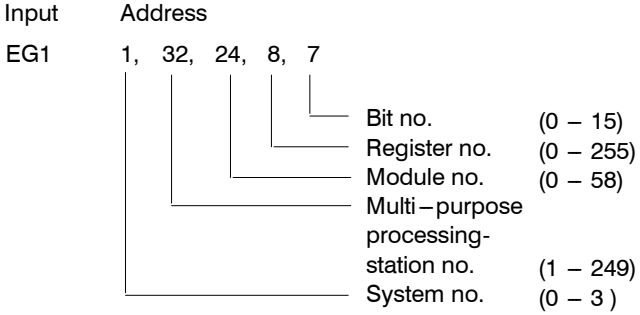
The allocation of module input and output signals to the respective registers of the shared memory is determined by user data entered via the PDDS.

The user entries are made in the form of address lists.

### Address list for module inputs

In the address list for module inputs, each module input is assigned the source location or the associated process interface of the signal to be received.

For module inputs receiving their signals from the bus, addressing is done by allocating the source location address to EGn, e.g.:




For module inputs receiving their signal from the process interface, addressing is done by allocating the process interface to EGn, e.g.:


For module inputs receiving their signal from the process operator station (POS), addressing is done by allocating L to EGn, e.g.:


The address list for inputs is translated by the PDDS into two module–internal lists, the ”Bus address list” and the ”Allocation list Module inputs”.

For all telegrams to be used by the module, the bus address list contains the respective source addresses and sink registers.

Incoming telegrams whose addresses are included in the bus address list are written into the sink register of the shared memory. Incoming telegrams whose addresses are not included in the bus address list are ignored by the module.

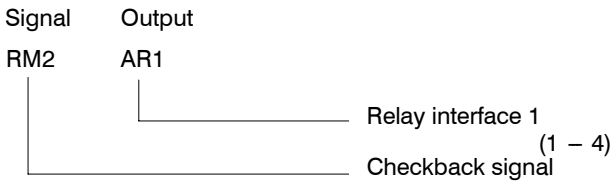
The allocation list for module inputs includes, for each module input, the associated sink register number and, in the case of binary values, also the bit position.

### Address list for module outputs to the bus

In the address list for module outputs, a source register is defined for each signal to be issued by the module. Additionally, a source bit is defined in the case of binary signals, e.g.:


### Addressing the process interface for the relay outputs

For module outputs supplying their signal to the relay interface, addressing is done in the structure list by allocating ARn, n denoting the number of the relay interface, e.g.:




### Address formation

The system and station addresses are set on the station–bus control module and are transmitted by this module to all other modules belonging to one multi–purpose processing station.

The module addresses are defined by the connections made on the backplane so that each module is automatically set to the assigned address when being plugged into its slot.

## Limit value list

The limit value list contains a set of 4 limit values for each one of a maximum of 16 function blocks GRE (limit signal formation for one analog value). It is stored in the EEPROM and – in the case of RAM operation – in the RAM.

Limit value lists can be changed at any time from the PDDS and POS using a ”job memory” (RAM). Changes are stored in the EEPROM in the case of EEPROM operation, and in the RAM in the case of RAM operation. When user lists are taken over from the RAM into the EEPROM, and vice versa, the limit value lists are also taken over.

## Parameter list

The parameter list contains up to 80 values for parameters of the function blocks. It is handled and stored in the same way as the limit value list.

## Simulation list

Using the PDDS, it is possible to simulate, at up to 32 module inputs, signals normally received via the bus, by overwriting them with constant values. This simulation list is handled and stored in the same way as the limit value list.

## Event generation

The module is requested by the PROCONTROL system once every cycle to transmit the information filed in the source registers of the shared memory.

If any values change during a cycle, this change will be treated as an event.

The module recognizes the following occurrences as events:

– Change of status in the case of binary values
– Change of an analog value by a permanently set threshold value of approx. 0.39 % and elapse of a time delay of 200 ms since the last transfer (cyclic or event–related).

If an event occurs, cyclic operation is interrupted and the new values are transferred to the bus with priority.

## Disturbance bit evaluation, reception monitoring

The telegrams supplied via the bus may be provided with a fault flag on bit position 0. This fault flag is generated by the source module on the basis of plausibility checks, and the disturbance bit is set to “1” in the event that specific disturbances are present (see Function Block Descriptions).

In order to be able to recognize errors during signal transfer, the module also incorporates a feature that monitors the input telegrams for cyclic renewal. If a telegram has not been renewed within a certain time (e.g. due to failure of the source module), bit 0 is set to ”1” in the allocated sink register of the shared memory. In binary value telegrams, all the binary values are simultaneously set to “0”. In the case of analog values, the previous value is retained.

A set disturbance bit does not automatically involve a reaction in the sink module. If the disturbance bit of a telegram is to be evaluated, provision must be made for this during structuring.

In the ”Binary control” and ”Analog control” modes, disturbance bits of received telegrams can only be used within the module. They are not included in telegrams which are to be transmitted.

In the ”Signal conditioning” mode, disturbance bits are also included in transmitted telegrams.

## Diagnosis and annunciation functions

**Disturbance annunciations on the module**

The light–emitting diodes on the module front are used for the following annunciations:

| | Designation of LED |
|---|---|
| – Disturbance | ST |
| – Module disturbance | SG |

Light–emitting diode ST signals all disturbances of the module and of data communication with the module.

Light–emitting diode SG signals module disturbances only.

**Disturbance annunciation signals to the alarm annunciation system**

The alarm annunciation system and the control diagnostic system (CDS) receive disturbance annunciation signals from the control module via the bus.

**Diagnosis**

The incoming telegrams, the generation of telegrams to be transmitted, and internal signal processing are monitored for errors in the processing section of the module (self–diagnosis).

In the event of a disturbance, the type of disturbance is filed in the diagnostic register and, at the same time, a general disturbance annunciation is signalled to the PROCONTROL system.

When prompted, the module transfers a telegram containing the data stored in the diagnostic register (register 246) (see Fig.1).

The contents of the diagnostic register, the annunciations signalled via the general disturbance line, the annunciations on the CDS, and annunciation ST are shown in Fig. 1.

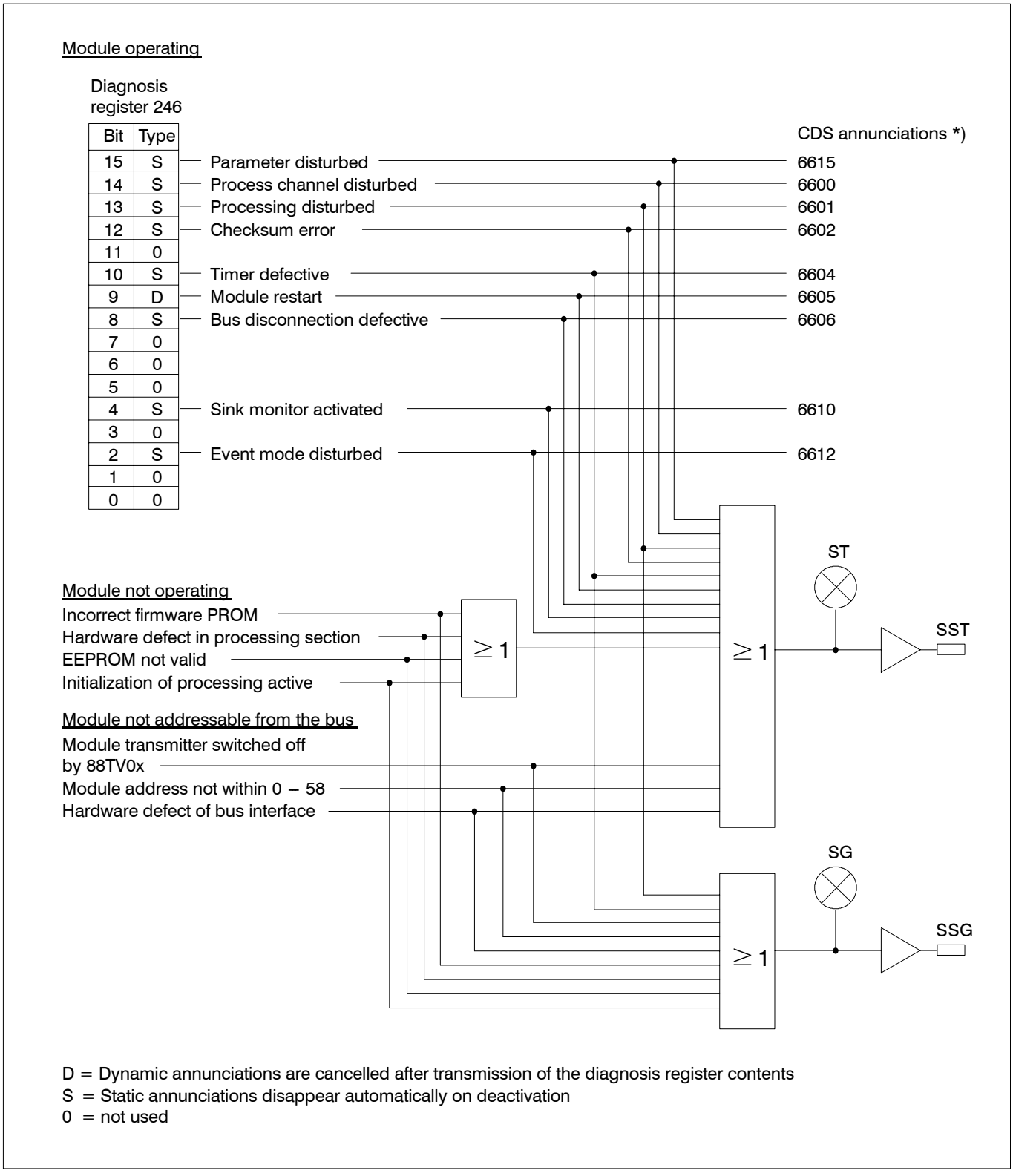



Figure 1: Diagnostic annunciations of 83SR04

The annunciation ”Process channel disturbed” may appear for the following reason:

– Short circuit at outputs US11...US41

*) The control diagnostic system (CDS) provides a description for every annunciation number. This description provides, among other data:

– Information on cause and effect of the disturbance
– Recommendations for its elimination.

This makes for fast elimination of disturbances.