Digital Input Processor and Digital Input Sequence of Events Processor MU-PDIX02/MU-PDIS12

FTAs with Removable Plug-In Isolators			
Parameter	**Specification**		
	24 Vdc FTA	**120 Vac FTA 125 Vdc FTA**	**240 Vac FTA**
FTA Models	**MU-TDID12, TDID52**	**MU-TDIA12, TDIA52**	**MU-TDIA22, TDIA62**
Input Channels	32	32	32
Accumulated Input Frequency	dc - 15 Hz	NA	NA
Galvanic Isolation (field to PM/APM/HPM)	1500 Vac rms or ±1500 Vdc(2)	1500 Vac rms or ±1500 Vdc	1500 Vac rms or ±1500 Vdc
Isolation Technique	Optical	Optical	Optical
Digital Input Pwr. Range(1)	20-30 Vdc	90-132 Vac rms	180-264 Vac rms
Sense Current (ON condition)	4.5 mA minimum	3.5 mA minimum	2.2 mA minimum
Sense Current (OFF condition)	2.8 mA maximum	1.5 mA maximum	1.0 mA maximum
Pick Up Voltage (ON condition)	20 Vdc minimum(3)	90 Vac rms minimum(4)	180 Vac rms minimum(4)
Drop Out Voltage (OFF condition)	10 Vdc maximum(3)	25 Vac rms maximum(4)	50 Vac rms maximum(4)
Absolute Delay Across Input Filter and Isolation (Bounceless Input to PM/APM/HPM logic level change)	2.0 ms maximum	25 ms maximum	25 ms maximum
Frequency Range	dc	47-63 Hz	47-63 Hz
Surge withstand capability	ANSI/IEEE C37.90.1-1978	ANSI/IEEE C37.90.1-1978	ANSI/IEEE C37.90.1-1978

(1) These dc voltage limits include an ac component that has a peak value of 5% of the nominal dc range value.
(2) Not applicable if system power is used to power field inputs.
(3) This voltage present from '-' terminal to ground.
(4) The voltage present across input terminals.

(Continued)

Digital Input Processor and Digital Input SOE Processor (continued) **MU-PDIX02/ MU-PDIS12**

Packaged FTAs without Plug-In Isolators		
Parameter	**Specification**	
	24 Vdc FTA	**120 Vac FTA**
FTA Model Numbers	**MU-TDID72**	**MU-TDIA72**
Input Channels	32	32
Accumulated Input Frequency	dc - 15 Hz	NA
Galvanic Isolation (field to APM)	1500 Vac rms or ±1500 Vdc(5)	1500 Vac rms or ±1500 Vdc
Isolation Technique	Optical	Optical
Digital Input Pwr. Range(1)	18-30 Vdc	90-132 Vac rms
Sense Current (ON condition)	12 mA minimum	5.2 mA minimum
Sense Current (OFF condition)	4.3 mA maximum	1.47 mA maximum
Absolute Delay Across Input Filter and Isolation (Bounceless Input to PM/APM/HPM logic level change)	3.6 ms maximum	25 ms maximum
Field Resistance for Guaranteed ON condition(2, 3)	100 Ω maximum	100 Ω maximum
Field Resistance for Guaranteed OFF condition(2, 3)	45 kΩ minimum(4)	71 kΩ minimum
Frequency Range	dc	47-63 Hz
Surge withstand capability	ANSI/IEEE C37.90.1-1978	ANSI/IEEE C37.90.1-1978

(1) These dc voltage limits include an ac component that has a peak value of 5% of the nominal dc range value.

(2) This resistance is present between the two legs of a DI current sense circuit.

(3) For field wiring distance guidelines, see the appropriate *Site Planning* manual.

(4) Reduce to 37.4 kΩ if digital input power range is limited to 18-25 Vdc.

(5) Not applicable if system power is used to power field inputs.

Digital Input Processor Redundancy Option (MU-PDIS12 Only)

Parameter	Specification
Input Scan Cycles Missed or Delayed During Swap or Failover	No cycles missed or delayed (all FTA types)