Format:

- dig_discrep_val=xx
- Default = 250 (e.g. 250/512 volts or 512 mV for T8403).

**di120vac_discrep_val**

The value is specified as 100 counts per volt. It specifies the allowed difference between voltage readings of T8424 Digital Input channel slices before the TMR Processor indicates a Channel Discrepancy.

Changes to this value are not implemented until the TMR Processor is rebooted after the download of the System.INI file.

Format:

- di120vac_discrep_val=xx
- Default = 500 (500/100 volts or 5 V).

**do_discrep_val**

The value is specified in counts per volt and matches the module voltage reading scale. It specifies the allowed difference between voltage readings of Digital Output channel slices before the TMR Processor indicates a Channel Discrepancy. This setting is used in all Digital Output Modules and T8449.

Changes to this value are not implemented until the TMR Processor is rebooted after the download of the System.INI file.

Format:

- do_discrep_val=xx
- Default = 1000 (e.g. 1000/500th volts or 2 V for T8451).

**ao_discrep_val**

The value is specified as 500 counts per volt. It specifies the allowed difference between voltage readings of Analogue Output channel slices before the TMR Processor indicates a Channel Discrepancy.

This applies to T8480 analogue output modules only.

Changes to this value are not implemented until the TMR Processor is rebooted after the download of the System.INI file.

Format:

- ao_discrep_val=xx
- Default = 250 (250/500 volts or 500 mV).

**zim_discrep_val**

The value is specified as 500 counts per volt. It specifies the allowed difference between voltage readings of Zone Interface Module inputs before the TMR Processor indicates a Channel Discrepancy.

This applies to T8448 ZIM Modules (input channels only).

Changes to this value are not implemented until the TMR Processor is rebooted after the download of the System.INI file.

Format:

- zim_discrep_val=xx
- Default = 200 (200/500 volts or 400 mV).

**smm_discrep_val**

The value is specified as rpm. It specifies the allowed difference between rpm measurements on a T8442 Speed Input channel set before the TMR Processor indicates a Channel Discrepancy.

This applies to T8442 Speed Monitor Modules (input channels only).

Changes to this value are not implemented until the TMR Processor is rebooted after the download of the System.INI file.

Format:

- smm_discrep_val=xx
- Default = 10 rpm.

**Note**: That there is no discrepancy checking on a T8444.

### 3.1.5. ISaGraf Configuration Section

IsaGraf processing cycles take priority within the Processor. The IsaGraf Sleep Period is the time frame between IsaGraf cycles. It is the period used for scanning the Trusted Communication Interface Modules, but it only applies when these are the only modules in the system and no other modules are present. The value entered here must be sufficient to allow all the Communication Interfaces used in the Trusted System to be scanned. As a rule of thumb, a minimum of 32 ms must be entered.

The default value for the Maximum Scan Time is 1000 ms. The value entered must be less than the Process Safety Time allocated to the Trusted System for the Plant, but greater than the scan time of the application program. If the value set is exceeded by the application program scan, the Trusted System will shutdown to its fail safe state. Note that Processor hot swaps and online updates can significantly extend the scan time, and it is recommended to set the maximum scan time to approximately four times the ‘current’ scan time as displayed in the Toolset Debugger Window.

### 3.1.6. Chassis Section

The figure entered against Max Racks is the number of chassis that will be used in the System and must include the Controller Chassis plus any local and / or remote Expander Chassis.

### 3.1.7. InterRange Instrumentation Group (IRIG)

Later versions of the TMR Processor are able to receive InterRange Instrumentation Group (IRIG) signals. For this to be active, the Processor Interface Adapter Unit (IRIG-B, model T8121 or T8123) must be fitted to the rear of the Controller Chassis. This contains the IRIG-B 'dongle'. The Check to Enable box in the InterRange Instrumentation Group (IRIG) area of the display must be selected. The user may also select which mode (IRIG-B002 or IRIG-B122) is required and also enable LED monitoring. If LED Monitoring is selected, the User 2 LED on the Front Panel of the Processor will flash to indicate that a valid IRIG signal is detected (once per second).

IRIG-B122 is the 1 - kHz amplitude modulated version of the signal.

IRIG-B002 is the RS485/422 version of the signal.

Note that configuring the above system configuration options and fitting/wiring the appropriate adapter unit is all that is required to ensure that the IRIG signals are assigned to the system clock. There is no need to add any programming to manipulate the Main Processor (MP) complex I/O definition boards TTMRP_3, TTMRP_4 and TTMRP_5 to synchronise the time. However, the IRIG signal does not contain any year information, and so an initial approximate setting of the real time clock will be necessary to enter the correct year.

The IRIG time source needs to be set up to output the same IRIG code as the TMR Processor is set up to receive. Some IRIG sources will output IRIG-B002 as TTL levels. This will not work with the TMR Processor, so ensure that the IRIG source is set to IRIG-B002 at 485/422 levels.

Some IRIG sources will have IRIG-B123 or B003 outputs. These have the time encoded in Straight Binary Seconds (SBS) at the end of the usual B122/002 message. These can be used with the TMR Processor because it ignores the SBS part of the message if there is one.

With the TMR Processor and the IRIG source set correctly, the time should be updated from the IRIG source once the module has booted. If the TMR Processor is not decoding the IRIG signal correctly for whatever reason, the System Health LED will flash red and the following will appear in the MP log:

```
48 IRIG: Maximum update interval exceeded
```

Typing `IRIG S` from the MP diagnostics will list the status of the IRIG Port.